FIG. 1

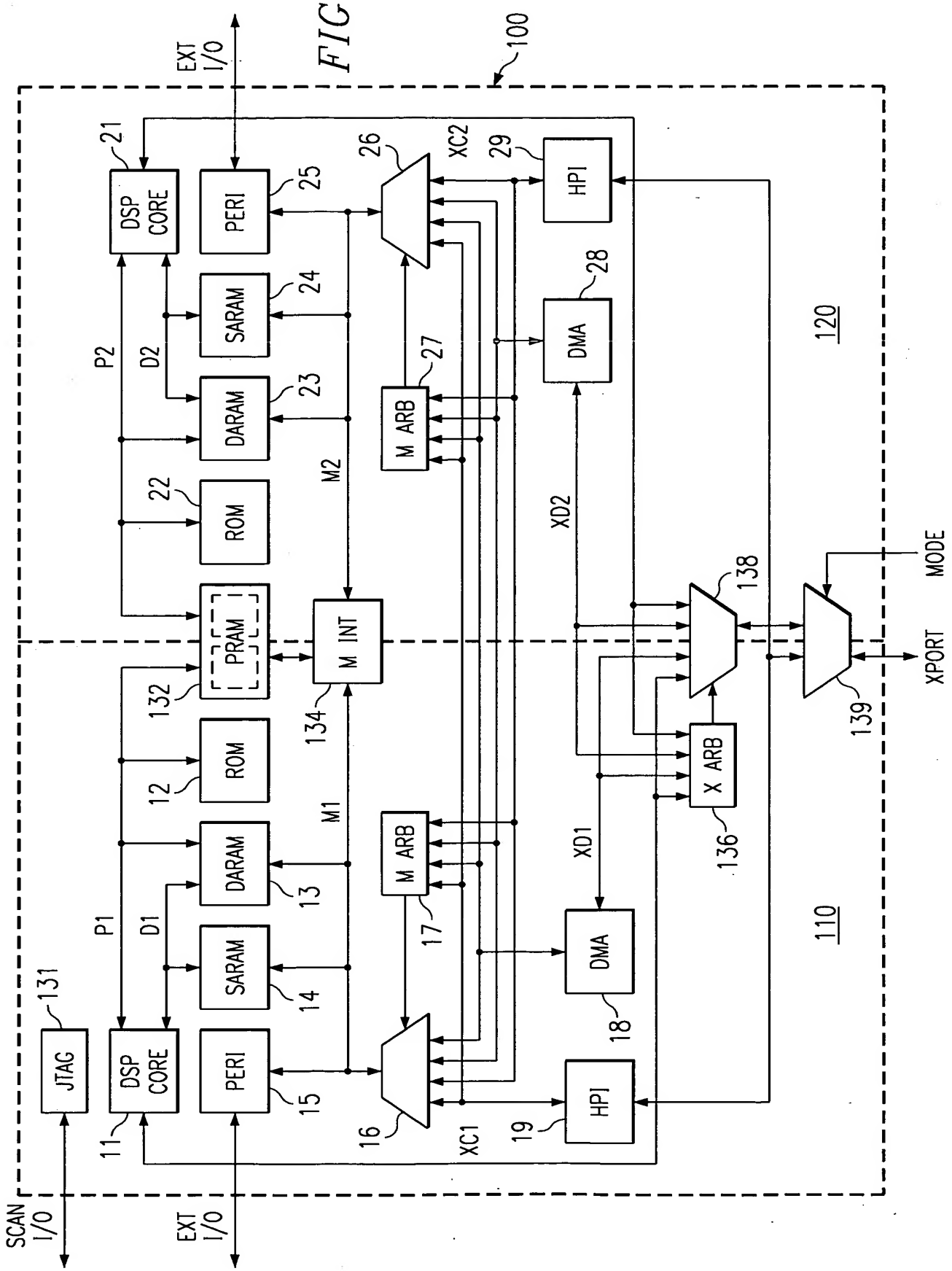
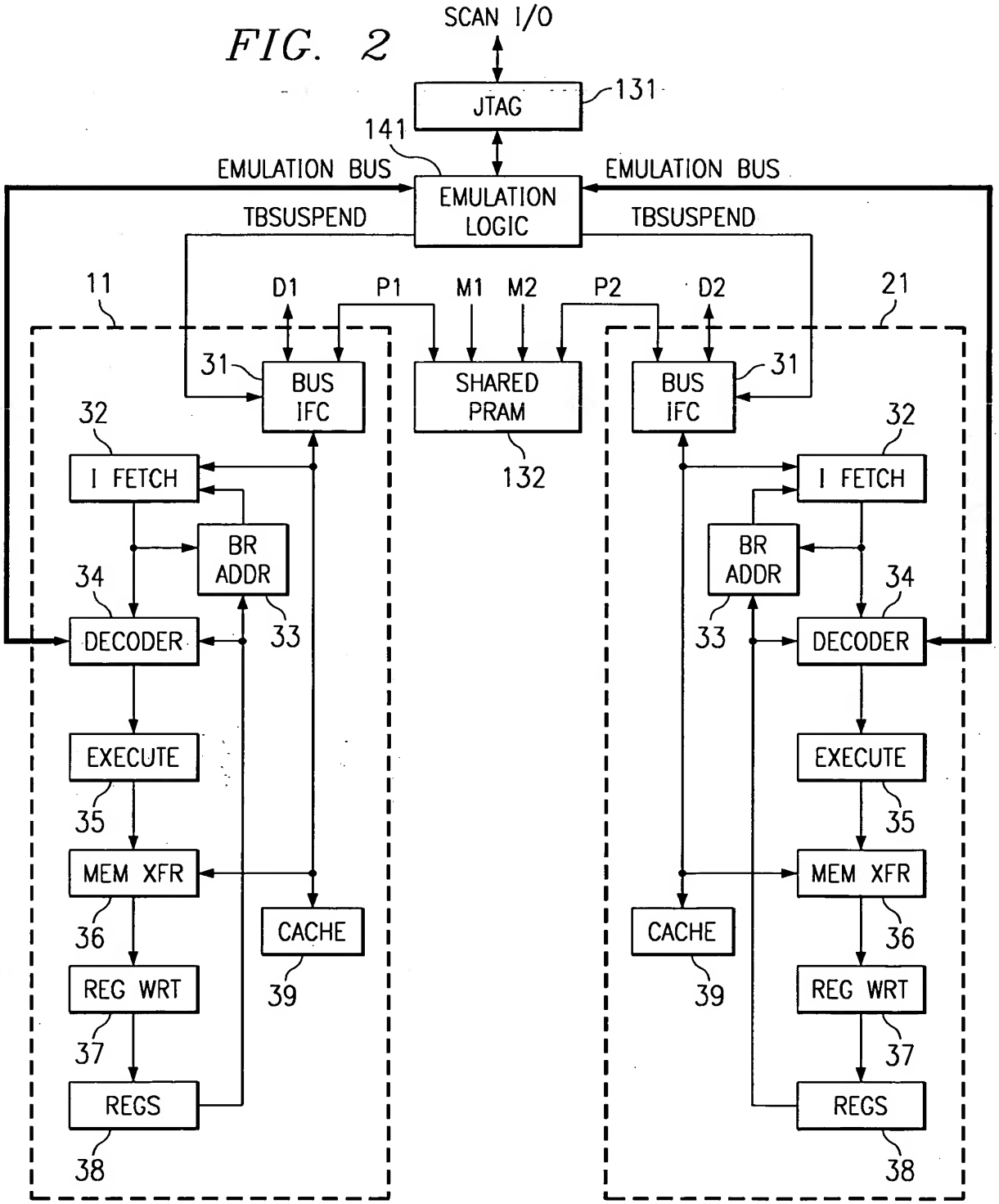

100
EXT I/O
DSP CORE
PERI
SARAM
DARAM
ROM
PRAM
JTAG
SCAN I/O
EXT I/O
P1
P2
D1
D2
M1
M2
M INT
M ARB
DMA
HPI
X ARB
XC1
XC2
XD1
XD2
MODE
XPORT
110
120
11
12
13
14
15
16
17
18
19
21
22
23
24
25
26
27
28
29
131
132
134
136
138
139

FIG. 2


SCAN I/O
JTAG
131
141
EMULATION BUS
EMULATION LOGIC
EMULATION BUS
TBSUSPEND
TBSUSPEND
11
21
D1
P1
M1
M2
P2
D2
31
BUS IFC
SHARED PRAM
132
BUS IFC
31
32
I FETCH
BR ADDR
34
DECODER
33
EXECUTE
35
MEM XFR
36
CACHE
39
REG WRT
37
REGS
38
32
I FETCH
BR ADDR
33
34
DECODER
EXECUTE
35
MEM XFR
CACHE
36
39
REG WRT
37
REGS
38

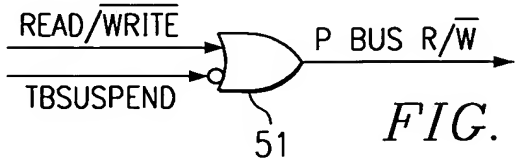

READ/WRITE
TBSUSPEND
P BUS R/W
51

FIG. 3